Claims

What is claimed is:

1. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel in a direct access storage device (DASD) comprising:

an acquisition timing circuit for generating an acquisition timing signal;

said acquisition timing circuit including a plurality of compare functions for receiving and comparing consecutive input signal samples on an interleave with a threshold value;

said acquisition timing circuit including a majority rule voting function coupled to said plurality of compare functions for selecting a timing interleave.

2. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 1 wherein said acquisition timing circuit includes three compare functions for receiving and comparing three consecutive input signal samples on said interleave with said threshold value.

3. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 2 wherein said majority rule voting function includes a two of three voting function coupled to said plurality of compare functions for selecting said timing interleave.

4. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 1 further includes tracking timing circuitry for generating a timing error signal during a read operation.

5. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 4 wherein said tracking timing circuitry includes a channel data detector, said channel data detector receiving disk signal input samples and including a multiple-state path memory.

6. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 5 wherein said tracking timing circuitry further includes a low latency detector receiving disk signal input samples.

7. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 6 wherein said tracking timing circuitry further includes a selector function coupled to an output of said low latency detector and coupled to said multiple-state path memory for selecting a state and utilizing said low latency detector output to select a state of said path memory and said selector function providing a low latency output corresponding to said selected state.

8. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 7 wherein said low latency output is used for generating said timing error signal during a read operation.

9. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 7 wherein said low latency output is applied to a convert-to-estimated sample function for generating an estimated sample and said estimated sample subtracted from said disk signal input samples for generating said timing error signal during a read operation.

10. A method for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel in a direct access storage device (DASD) comprising the steps of:

receiving and comparing multiple consecutive input signal samples on an interleave with a threshold value;

applying a majority rule voting function and selecting a timing interleave for an acquisition timing signal;

during a read operation, applying disk signal input samples to a channel data detector and to a low latency data detector; said channel data detector including a multiple-state path memory;

utilizing an output of said low latency detector for selecting a state of said multiple-state path memory and providing a low latency output corresponding to said selected state; and

utilizing said low latency output for generating said timing error signal during said read operation.

11. A method for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 10 wherein the step of receiving and comparing multiple consecutive input signal samples on an interleave with a threshold value includes the step of receiving and comparing three consecutive input signal samples on said interleave with said threshold value.

12. A method for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 11 includes the step of identifying a zero or a one value for said three consecutive input signal samples.

13. A method for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 10 wherein the step of applying a majority rule voting function and selecting a timing interleave for an acquisition timing signal includes the step of applying a two out of three voting function and selecting said timing interleave for said acquisition timing signal.

14. A method for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 10 wherein the step of utilizing an output of said low latency detector for selecting a state of said multiple-state path memory and providing a low latency output corresponding to said selected state includes the step of selecting a low latency state of said multiple-state path memory and providing said low latency output.

15. A method for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 10 wherein the step of utilizing said low latency output for generating said timing error signal during said read operation includes the steps of converting said low latency output to an estimated sample output and subtracting said estimated sample output from said disk signal input samples for generating said timing error signal during said read operation.

16. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel in a direct access storage device (DASD) comprising:

tracking timing circuitry for generating a timing error signal during a read operation; said tracking timing circuit including a channel data detector, said channel data detector receiving disk signal input samples and including a multiple-state path memory;

said tracking timing circuit including a low latency detector receiving disk signal input samples;

said tracking timing circuit including a selector function coupled to an output of said low latency detector and coupled to said multiple-state path memory for selecting a state and said selector function utilizing said low latency detector output for selecting said state of said path memory and for providing a low latency output corresponding to said selected state; and

said low latency output being used for generating said timing error signal during a read operation.

17. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 16 includes a convert-to-estimated sample function receiving said low latency output and generating an estimated sample and said estimated sample subtracted from said disk signal input samples for generating said timing error signal during a read operation.

18. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 16 wherein said low latency detector includes a 4-state Viterbi detector.

19. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 16 wherein said low latency output is less than a latency of an output of said channel data detector.

20. Apparatus for enhanced timing loop for a partial-response maximum-likelihood (PRML) data channel as recited in claim 16 includes an acquisition timing circuit for generating an acquisition timing signal; said acquisition timing circuit including a plurality of compare functions for receiving and comparing consecutive input signal samples on an interleave with a threshold value, and a majority rule voting function coupled to said plurality of compare functions for selecting a timing interleave.